CET246 Electronic Design Automation
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Laboratory Exercise #5: Netlist Creation

What to do:

1) Unzip the example project into a directory which you have write access to.
2) Open KiCad
3) Open the example project
4) Open the Schematic in Eeschema (within KiCad)
5) From Eeschema run CvPcb and associate footprints with the appropriate part designation
6) From Eeschema re-generate the netlist in the 'Pcbnew' format
7) Run Pcbnew from the toolbar in EESchema
8) Import the netlist in Pcbnew from the toolbar
9) Arrange the components
10) Make all traces necessary to remove the ratnest. Use the appropriate layers
11) Draw the board edge on the **Edge Cuts** layer. The board shall be no larger than 60 sq. in.
12) Include mounting holes
13) Run DRC (bug) check with default design rules and resolve all errors
14) Generate all gerber, drill, and map files as done in the previous lab

What to turn in:

1) A single zip file with all PCB, library, gerber, drill, and map files. Name the file according to this format:

   Course_Semester_YourLastName_Lab##.zip

   So I would name my file:

   CET246_Fall2018_Broderick_Lab05.zip

